REMARKS

The Office Action dated March 10, 2006 in this Application has been carefully considered. Claims 1-2, 4-6, 8-11, 13-15, 17-20, 22-24, and 26-27 are pending. The above amendments and the following remarks are presented in a sincere attempt to place this Application in condition for allowance. Claims 1-2, 4, 8, 10-11, 13-14, 17, 19-20, 22, and 26 have been amended in this Response. Claims 3, 7, 12, 16, 21, and 25 have been cancelled in this Response. Reconsideration and allowance are respectfully requested in light of the above amendments and following remarks.

Claims 1, 10, and 19 stand rejected under 35 U.S.C. §102(b) and §103(a) by U.S. Patent Publication No. 2002/0144079 by Willis et al. ("Willis"). Insofar as they may be applied against the Claims, these rejections are traversed and overcome.

Regarding Claims 1, 10, and 19, Willis was cited as assertedly fully disclosing the following: "a method and/or apparatus for sharing translation look-aside buffer (TLB) entries among multiple logical processors (ergo multiple concurrent threads of execution within a single physical multi-threaded processor) comprising a valid indicator for each concurrent thread of execution along with a single virtual/effective address tag and corresponding physical/real address for each TLB entry, such that such entries may be maintained by computer program code to be consistent with the defined address mapping of said multiple threads of execution." Office Action, at Page 2 (*citing* Willis, Abstract, FIGS. 7a-b, 9a-c, paragraphs 52, 61, and Claim 35). Further, the Examiner stated, "Any limitation not otherwise considered explicitly addressed is considered correspondingly clearly inherent in that taught, obvious to one of ordinary skill in the art, and/or not sufficient to patentably distinguish over prior art." Office Action, at Pages 2-3.

Rejected independent Claims 1, 10, and 19 as now amended more particularly recite some of the distinguishing characteristics of the present invention, namely, "upon determining that the

matching entry is not marked valid for the first thread but is marked valid for other threads, determining whether the information in the matching entry is correct for the first thread" and "upon determining that the information in the matching entry is correct for the first thread, setting a valid indicator marking the entry as valid for the first thread." Support for this Amendment can be found, among other places, at Page 3, lines 12-21, and Page 8, line 32 through Page 9, line 13 of the original Application.

First, Applicants respectfully note that nowhere does Willis disclose, teach, or suggest "storing an effective address (EA) used by a thread in an Effective to Real Address Translation (ERAT) table," as recited by Claims 1, 10, and 19. Instead, Willis teaches, "a mechanism for sharing among multiple logical processors, a translation lookaside buffer (TLB) to translate *virtual addresses*, for example into physical addresses." Willis, paragraph [0021] (emphasis added). Nowhere does Willis even hint at *effective addresses*. As such, Willis clearly does not teach each and every element of amended Claims 1, 10, and 19, and therefore, cannot be said to anticipate the amended Claims. Accordingly, Applicants respectfully request that the rejections of Claims 1, 10, and 19 under 35 U.S.C. §102(b) be withdrawn.

Neither does Willis suggest, teach, or disclose "upon determining that the matching entry is not marked valid for the first thread but is marked valid for other threads, determining whether the information in the matching entry is correct for the first thread" or "upon determining that the information in the matching entry is correct for the first thread, setting a valid indicator marking the entry as valid for the first thread." Instead, Willis teaches:

> [I]f a processor initiates a TLB request to look up a virtual address translation and the TLB entry in latches 633 and 637 contains an ASID that matches the ASID for the virtual address to be translated, and further if the entry contains a VAD that matches the VAD for the virtual address, and finally if sharing indication 619 indicates a set of logical processes including one associated with the processor initiating the TLB request, then the entry in latch 633 and latch 637 may be used

> to translate the virtual address. Otherwise, control logic 604 may initiate installation of a new virtual address translation entry for TLB 602.

Willis, Paragraph [0037]. That is, if the TLB ASID matches, and the VAD matches, and the sharing indication indicates that the processor can share in this address, then that entry is used to validate the address; otherwise, a new entry is put in the TLB. Further, "If a processor . . . initiates a TLB request to installation of a new virtual address translation entry, then TLB 602 may be searched for any existing entries that can be shared." Willis, Paragraph [0039]. That is, in the additional situation where a processor requests a new TLB entry, the TLB can be searched to see if the requested address is in the TLB and can be shared. If the TLB entry exists and can be shared, it is used, otherwise, a new entry is provided.

This is one of the identified problems that are solved by the present invention. Referring to the existing technology, the Background of the Specification recites:

> Note that in the case where there is a valid EA to RA mapping in the ERAT table, but the thread identifier is not set for the thread requesting the EA lookup, a new entry will be added. This wastes valuable resources because (i) each thread will have its own entry in the ERAT table for the same valid EA to RA mapping, creating otherwise duplicate entries that differ only in terms of the thread identifier and (ii) a secondary translation must be performed on the EA to retrieve an RA, and the secondary translation operation is much slower than an ERAT table lookup.

Specification, Page 2, lines 19-29. Instead, amended Claims 1, 10, and 19 recite, "upon determining that the matching entry is not marked valid for the first thread but is marked valid for other threads, determining whether the information in the matching entry is correct for the first thread" and "upon determining that the information in the matching entry is correct for the first thread, setting a valid indicator marking the entry as valid for the first thread." Thus, not only does Willis teach a different mechanism than that recited in the amended independent Claims, the Willis system is expressly rejected by the novel invention recited in the amended independent Claims.

In view of the foregoing, it is apparent that the cited reference does not disclose, teach or suggest the unique combination now recited in amended Claims 1, 10, and 19. Applicants therefore submit that amended Claims 1, 10, and 19 are clearly and precisely distinguishable over the cited reference in a patentable sense, and are therefore allowable over this reference and the remaining references of record. Accordingly, Applicants respectfully request that the rejections of amended Claims 1, 10, and 19 under 35 U.S.C. §102(b) and §103(a) be withdrawn and that Claims 1, 10, and 19 be allowed.

Claims 2-9, 11-18, and 20-27 stand rejected under 35 U.S.C. §103(a) by Willis in view of U.S. Patent No. 5,680,566 by Peng et al. ("Peng"). Insofar as they may be applied against the Claims, these rejections are traversed and overcome.

Regarding Claims 2-9, 11-18, and 20-27, Willis was cited as assertedly "considered to explicitly and/or inherently implicitly teach the entirety [sic] the claimed invention." Office Action, at Page 3. As described above, Applicants respectfully traverse that assertion. Additionally, however, Peng was cited as assertedly fully disclosing, "a system and/or method comprising a TLB such that it may be determined if multiple TLB entries exist for a given virtual/effective addresses, and further that such an existing entry may be utilized *as the basis of an updated TLB entry* for differing process/thread's entry, although thereby inherently invalidating the previous process and/or thread entry's physical/real address mapping with one looked up in a secondary virtual-to-physical address table." Office Action, at Page 3 (citing Peng, abstract, col. 3-4, lines 49-9)(emphasis added). The Examiner further stated that it would have been obvious to combine the teachings of Willis and Peng, "for the benefit of enabling the use a single TLB entry for multiple concurrent threads which have been determined to have identical virtual-to-physical address

mappings as defined in such a secondary table associated with each process/thread." Office Action, at Page 3.

As described above, rejected independent Claims 1, 10, and 19 as now amended recite, "upon determining that the matching entry is not marked valid for the first thread but is marked valid for other threads, determining whether the information in the matching entry is correct for the first thread" and "upon determining that the information in the matching entry is correct for the first thread, setting a valid indicator marking the entry as valid for the first thread."

Applicants have demonstrated above that Willis fails to teach, disclose, or suggest the combination recited in Claims 1, 10, and 19. Neither does Peng teach, suggest, or disclose, "upon determining that the matching entry is not marked valid for the first thread but is marked valid for other threads, determining whether the information in the matching entry is correct for the first thread" and "upon determining that the information in the matching entry is correct for the first thread, setting a valid indicator marking the entry as valid for the first thread."

First, the Examiner's own characterization of Peng teaches away from the recited combination in Claims 1, 10, and 19. Specifically, the Examiner cited Peng as showing "an existing entry may be utilized *as the basis of an updated TLB entry.*" Office Action, at Page 3 (emphasis added). The claimed invention recites, "setting a valid indicator marking the entry as valid for the first thread" not deleting the entry and/or utilizing the entry as the basis of updating another entry. For at least this reason, Peng teaches away from the claimed invention.

Further, Peng expressly teaches a system/method that is incompatible with the invention as claimed in amended Claims 1, 10, and 19. Specifically, Peng teaches:

> The TLB is initially searched for a translation for a specified input address. If exactly one valid entry of the TLB stores a translation for the specified input address then the output address corresponding to the specified input address is determined from the contents of that entry. If two or more valid entries of the

> TLB store a translation for the specified input address then these entries are invalidated. The translation table is searched for a translation for the specified input address if more than one, or none, of the valid entries of the TLB store a translation of the specified input address.

Peng, col. 3, lines 56-65. Thus, in Peng, a TLB lookup that shows two or more valid entries results in invalidating both entries. By contrast, in the present invention avoids multiple valid entries through the claimed mechanism, "upon determining that the matching entry is not marked valid for the first thread but is marked valid for other threads, determining whether the information in the matching entry is correct for the first thread," as recited in amended Claims 1, 10, and 19.

Further, nowhere does Peng even mention determining whether a received effective address matches an ERAT entry indicating validity as to multiple threads. Instead, Peng merely seeks to avoid "errors of various sorts such as soft errors in RAM, hardware and transient errors and software errors" that result in causing "two or more translations for the same input address [to] appear in the TLB." Peng, col. 3, lines 23-32. As such, Peng seeks to eliminate multiple TLB entries, and does not address single entries that serve multiple threads.

Accordingly, Peng cannot be said to even approach teaching, disclosing, or suggesting, "setting a plurality of second thread valid indicators in the ERAT table entry for each thread using the EA to refer to the same RA," as recited in amended Claims 1, 10, and 19. As such, neither can Peng be said to teach, disclose, or suggest "upon determining that the matching entry is not marked valid for the first thread but is marked valid for other threads, determining whether the information in the matching entry is correct for the first thread" and "upon determining that the information in the matching entry is correct for the first thread, setting a valid indicator marking the entry as valid for the first thread," as recited in amended Claims 1, 10, and 19.

In view of the foregoing, it is apparent that the cited references do not disclose, teach or suggest the unique combination now recited in amended Claims 1, 10, and 19. Applicants therefore

submit that amended Claims 1, 10, and 19 are clearly and precisely distinguishable over the cited reference in a patentable sense, and are therefore allowable over this reference and the remaining references of record.

Claims 2, 4-6, and 8-9 depend on and further limit Claim 1. Claims 11, 13-15, and 17-18 depend on and further limit Claim 10. Claims 20, 22-24, and 26-27 depend on and further limit Claim 19. Hence, for at least the aforementioned reasons, Applicants respectfully submit that these claims are clearly and precisely distinguishable over the cited reference in a patentable sense, and are therefore also allowable over these references and the remaining references of record. As such, Applicants respectfully submit that these Claims would be deemed to be in condition for allowance. Accordingly, Applicants respectfully request that the rejections of dependent Claims 2, 4-6, 8-9, 11, 13-15, 17-18, 20, 22-24, and 26-27 under 35 U.S.C. §103(a) be withdrawn and that Claims 2, 4-6, 8-9, 11, 13-15, 17-18, 20, 22-24, and 26-27 be allowed.

Applicants have now made an earnest attempt to place this Application in condition for allowance. For the foregoing reasons and for other reasons clearly apparent, Applicants respectfully request full allowance of Claims 1-2, 4-6, 8-11, 13-15, 17-20, 22-24, and 26-27.

Applicants do not believe that any fees are due; however, in the event that any fees are due, the Commissioner is hereby authorized to charge any required fees due (other than issue fees), and to credit any overpayment made, in connection with the filing of this paper to Deposit Account No. 50-0605 of CARR LLP.

Should the Examiner deem that any further amendment is desirable to place this application in condition for allowance, the Examiner is invited to telephone the undersigned at the number listed below.

Respectfully submitted,

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